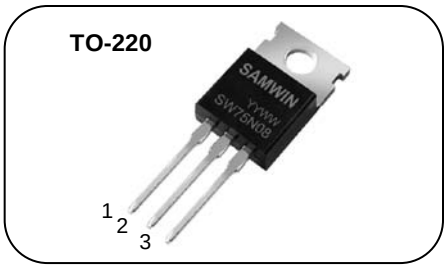
N-channel TO-220 MOSFET

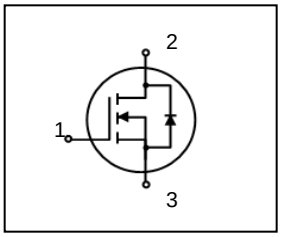
Features

- High ruggedness
- $R_{DS(ON)}$ (Max 11m Ω)@V_{GS}=10V
- Gate Charge (Typ 74nC)
- Improved dv/dt Capability
- 100% Avalanche Tested



1. Gate 2. Drain 3. Source

BV_{DSS} : 80V
I_D : 75A
$R_{DS(ON)}$: 11mΩ



General Description

This power MOSFET is produced with advanced VDMOS technology of SAMWIN. This technology enable power MOSFET to have better characteristics, such as fast switching time, low on resistance, low gate charge and especially excellent avalanche characteristics. This power MOSFET is usually used at high efficient DC to DC converter block and switch mode power supply.

Order Codes

Item	Sales Type	Marking	Package	Packaging
1	SW P 75N08	SW 75N08	TO-220	TUBE

Absolute maximum ratings

Symbol	Parameter		Value	Unit
V_{DSS}	Drain to Source Voltage		80	V
I_D	Continuous Drain Current (@T_C=25ºC)		75*	A
	Continuous Drain Current (@T_C=100ºC)		47*	A
I_{DM}	Drain current pulsed	(note 1)	300	A
V_{GS}	Gate to Source Voltage		±30	V
E_{AS}	Single pulsed Avalanche Energy	(note 2)	890	mJ
E_{AR}	Repetitive Avalanche Energy	(note 1)	160	mJ
dv/dt	Peak diode Recovery dv/dt	(note 3)	5	V/ns
P_D	Total power dissipation (@T_C=25ºC)		227	W
	Derating Factor above 25ºC		1.8	W/ºC
T_{STG}, T_J	Operating Junction Temperature & Storage Temperature		-55 ~ + 150	ºC
T_L	Maximum Lead Temperature for soldering purpose, 1/8 from Case for 5 seconds.		300	ºC

*. Drain current is limited by junction temperature.

Thermal characteristics

Symbol	Parameter	Value	Unit
R_{thjc}	Thermal resistance, Junction to case	0.55	ºC/W
R_{thcs}	Thermal resistance, Case to Sink	0.5	ºC/W
R_{thja}	Thermal resistance, Junction to ambient	56	ºC/W

Electrical characteristic (T_C = 25ºC unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Off characteristics						
BV_{DSS}	Drain to source breakdown voltage	V_{GS}=0V, I_D=250uA	80			V
ΔBV_{DSS} / ΔT_J	Breakdown voltage temperature coefficient	I_D=250uA, referenced to 25ºC		0.07		V/ºC
I_{DSS}	Drain to source leakage current	V_{DS}=80V, V_{GS}=0V			1	uA
		V_{DS}=80V, T_C=125ºC			50	uA
I_{GSS}	Gate to source leakage current, forward	V_{GS}=20V, V_{DS}=0V			100	nA
	Gate to source leakage current, reverse	V_{GS}=-20V, V_{DS}=0V			-100	nA
On characteristics						
$V_{GS(TH)}$	Gate threshold voltage	V_{DS}=V_{GS}, I_D=250uA	2.0		4.0	V
$R_{DS(ON)}$	Drain to source on state resistance	V_{GS}=10V, I_D = 40A		8.9	11	mΩ
Gfs	Forward Transconductance	V_{DS} =20V, I_D = 15 A	51			S
Dynamic characteristics						
C_{iss}	Input capacitance	V_{GS}=0V, V_{DS}=25V, f=1MHz		4700		pF
C_{oss}	Output capacitance			480		
C_{rss}	Reverse transfer capacitance			90		
$t_{d(on)}$	Turn on delay time	V_{DS}=45V, I_D=75A, R_G=25Ω (note 4, 5)		47	80	ns
tr	Rising time			93	150	
$t_{d(off)}$	Turn off delay time			112	200	
t_f	Fall time			77	150	
Q_g	Total gate charge	V_{DS}=60V, V_{GS}=10V, I_D=70A (note 4, 5)		74	140	nC
Q_{gs}	Gate-source charge			18		
Q_{gd}	Gate-drain charge			29		

Source to drain diode ratings characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_S	Continuous source current	Integral reverse p-n Junction diode in the MOSFET			75	A
I_{SM}	Pulsed source current				300	A
V_{SD}	Diode forward voltage drop.	I_S=75A, V_{GS}=0V			1.5	V
T_{rr}	Reverse recovery time	I_S=75A, V_{GS}=0V, dI_F/dt=100A/us		26		ns
Q_{rr}	Reverse recovery Charge			26		nC

※. Notes
1. Repeatitive rating : pulse width limited by junction temperature.
2. L = 0.32mH, I_{AS} = 75A, V_{DD} = 50V, R_G=25Ω, Starting T_J = 25ºC
3. I_{SD} ≤ 75A, di/dt = 100A/us, V_{DD} ≤ BV_{DSS}, Staring T_J =25ºC
4. Pulse Test : Pulse Width≤ 300us, duty cycle ≤ 2%
5. Essentially independent of operating temperature.

Fig. 1. On-state characteristics

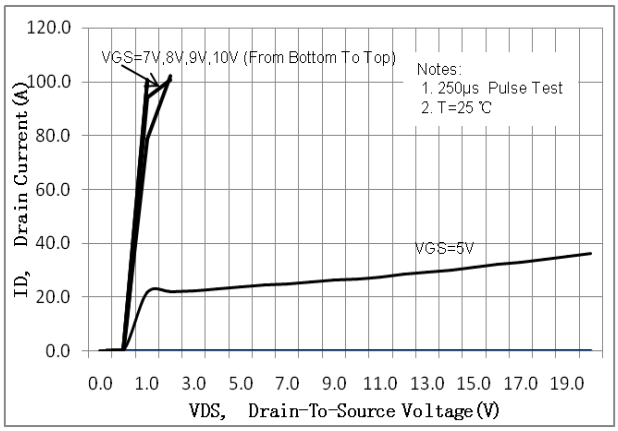


Fig. 2. On-resistance variation vs. drain current and gate voltage

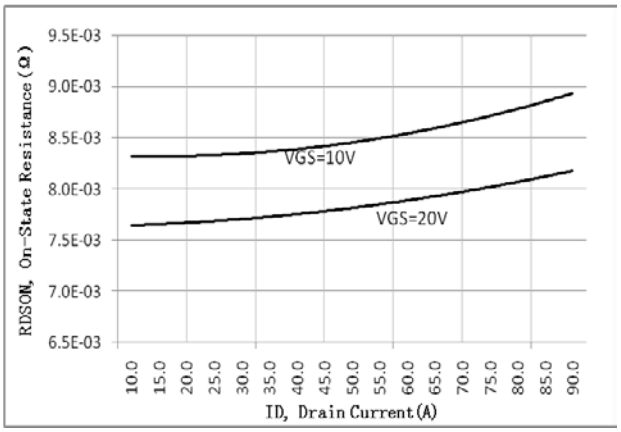


Fig. 3. Gate charge characteristics

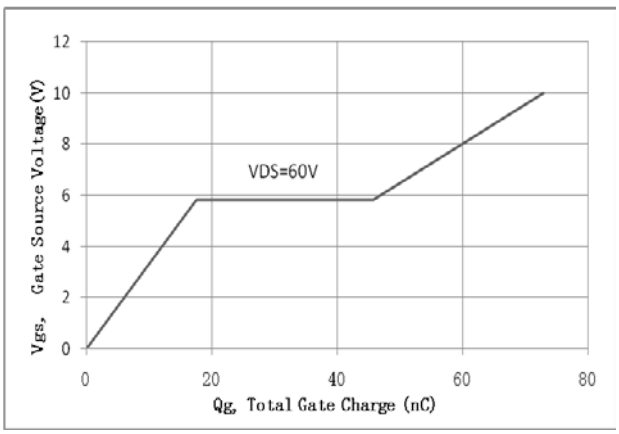


Fig. 4. On state current vs. diode forward voltage

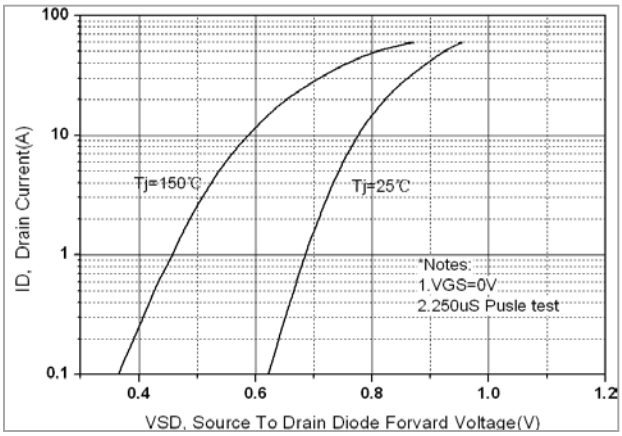


Fig 5. Breakdown Voltage Variation vs. Junction Temperature

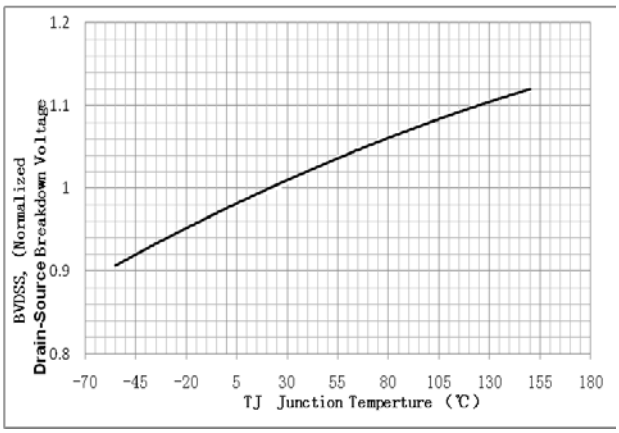


Fig. 6. On resistance variation vs. junction temperature

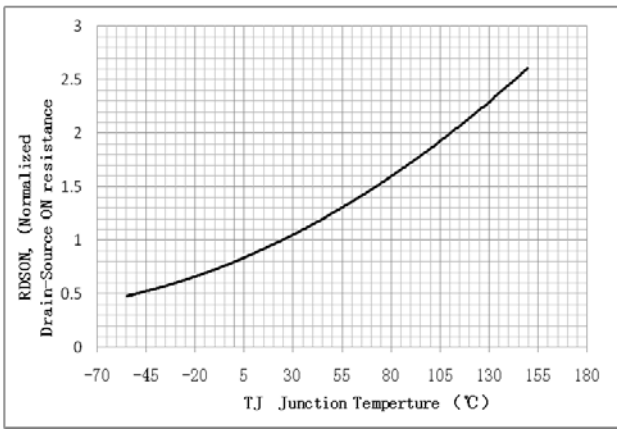


Fig. 7. Maximum safe operating area

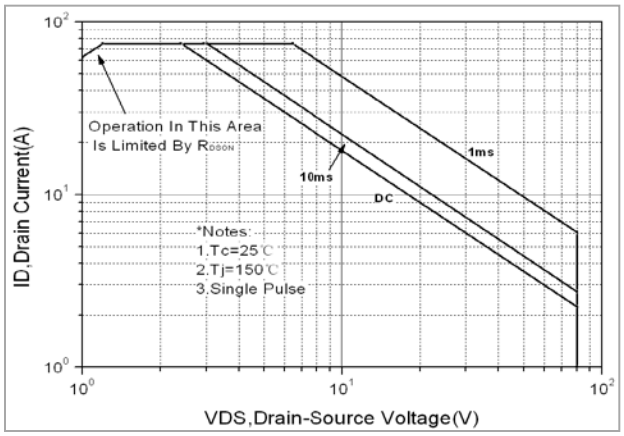


Fig. 8. Transient thermal response curve

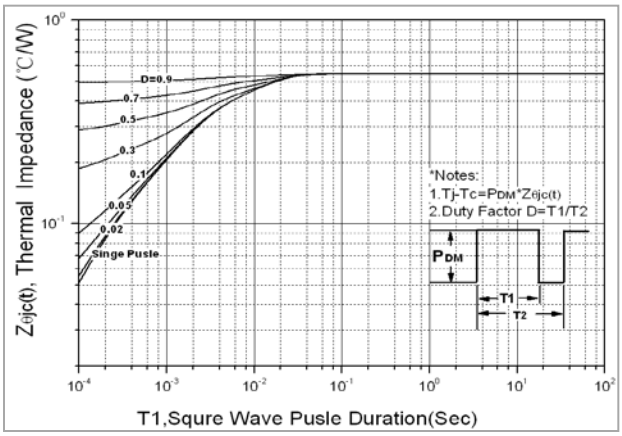


Fig. 9. Gate charge test circuit & waveform

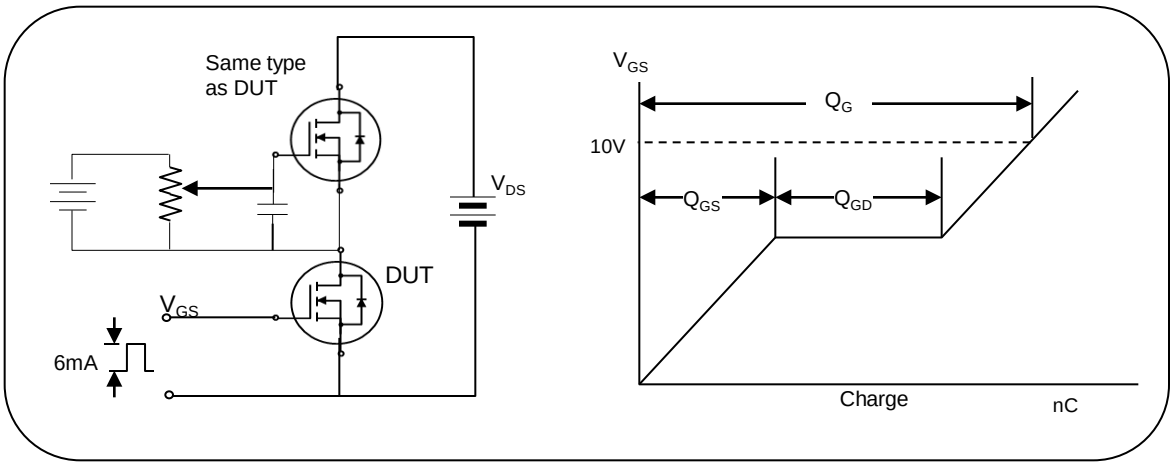


Fig.10. Switching time test circuit & waveform

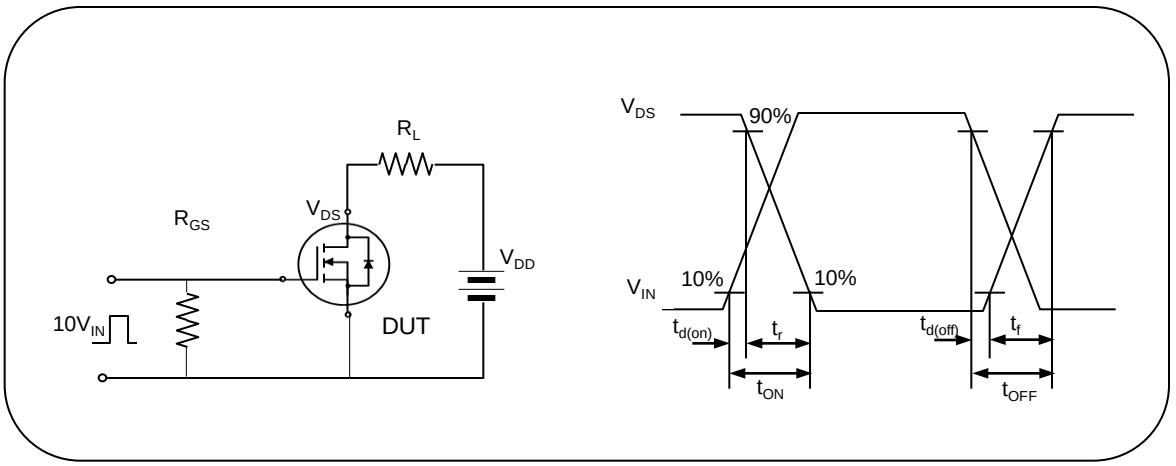


Fig. 11. Unclamped Inductive switching test circuit & waveform

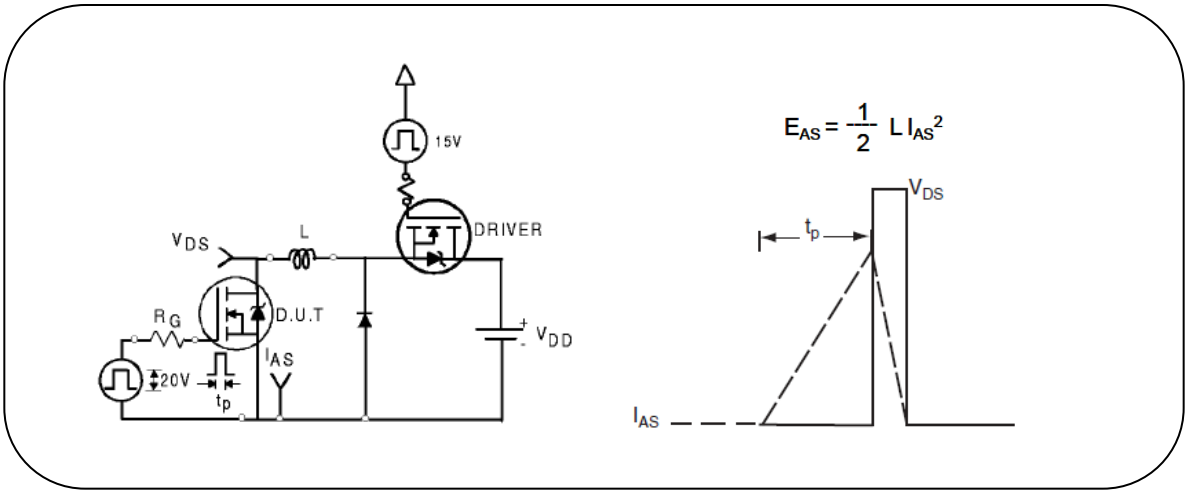


Fig.12 . Peak diode recovery dv/dt test circuit & waveform